REMARKS

With claims 4, 6, 8-9 and 29-36 pending, this response amends claims 4 and 36 as indicated in the remarks to follow.

Section 102 Rejection Based on Ohno

Claims 4 and 36 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ohno et al (U.S. Patent 5,091,692, hereinafter 'Ohno'). The Office Action states that Ohno in Fig 3 discloses a probe card assembly comprising a programmable controller (62) to control provision of test signals to test probes (7) of a probe card (6) for testing components on a wafer (2) wherein the programmable controller (62) is connected through the interface (14,15) to a test system controller (50), where the test system controller (50) provides test signals to the interface (15) to control testing of components on a wafer (2), wherein the interface (15) comprises one or more of a group consisting of wireless (optical interface). Based on the above amendments and the following remarks, rejection is respectfully traversed.

Claims 4 and 36 both claim "A probe card assembly comprising a programmable controller to control the provision of electrical test signals to test probes of the probe card for testing components on a device under test (DUT), wherein the programmable controller is connected through an interface to a test system controller, where the test system controller provides the test signals to the interface." In contrast, the programmable controller (62) of Ohno receives optical signals from the interface (15) to align the test probes (7) to pads (4) on the wafer (2), and does not provide electrical test

signals through the interface (15) to the probes (7). Optical signals provided from the test system controller (50) of Ohno are provided from a light source (40) connected to the tester (50), while electrical test signals are provided through probe card 6 from tester (50) that do not connect to the controller (62). Accordingly, claims 4 and 36 are believed allowable as not anticipated by Ohno under 35 U.S.C. § 102.

Section 102 Rejection Based on Miller

Claims 6, 8, and 29-32 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Miller et al (U.S. Patent Application No. 2004/0008024, hereinafter 'Miller').

Regarding claims 6, 8, 29 and 30, the Office Action states that Miller in Fig. 3 discloses a probe card assembly comprising a programmable controller (34,36) to control the provision of test signals to test probes (48) of a probe card for testing components on a wafer (42), wherein the programmable controller (34, 36) comprises a serial to parallel converter (connection of driver to node 50, at node 50 to the channel becoming parallel) configured to receive the test signals (TEST), the programmable controller (34, 36) configured to convert the test signal from serial to parallel and distribute the test signals in parallel to the test probes. This rejection is respectfully traversed.

Claims 6, 8 and 30 claim a probe card assembly with a serial to parallel converter to convert test signals and distribute the test signals to test probes. In Fig. 3 of Miller, the connection from node 50 to parallel resistors R2 (44) in the interconnect system 36 is not a serial to parallel converter. It is simply a distribution of a signal from a single line at point 50 to four parallel connected lines (44). If the single line is carrying a "serial"

signal, the "serial" data will not be converted to "parallel" data when provided on four separate lines 44, but instead will remain serial data. As indicated in the American Heritage Dictionary of English Language, 4th edition, 2000, the term "serial" for computers is "Of or relating to the sequential transmission of all bits of a byte over one wire: *a serial port; a serial printer.*" In contrast, according to the American Heritage Dictionary 4th edition, the term "parallel" refers to "Of or relating to the simultaneous transmission of all the bits of a byte over separate wires: *a parallel port; a parallel interface.* In Miller, no separation or combination of bits of a bite occur between point 50 and resistors 44. Miller further does not mention whether transmission of test data occurs in parallel or serial, or any serial to parallel conversion. Accordingly, claims 6, 8 and 30 are believed allowable as not anticipated by Miller.

Claims 29, 31 and 32, which claim a serial to parallel conversion, or serial transmission of test data are believed allowable as not anticipated by Miller based on the above arguments with respect to claims 6, 8 and 30.

Section 103 Rejection Based On Miller in view of Mori

Claims 33-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Miller in view of Mori et al (U.S. Patent Application No. 2002/0105352, hereinafter 'Mori'). The Office Action States that Miller discloses everything except for the probe card assembly of claim 8, wherein the serial to parallel converter comprises a serial digital to analog converter. The Office Action on the other hand indicates Mori in Fig. 2 teaches a probe card assembly with a digital to analog converter (61), and it would have been obvious to modify the teaching of Miller to use the DAC of Mori for the purpose of

converting the signals from analog form to digital form. This rejection is respectfully traversed.

Claims 33-35 claim conversion of serial digital signals to parallel analog signals for distribution to test probes. As indicated above in the remarks regarding the Section 102 rejection based on Miller, Miller does not disclose a serial to parallel conversion of test data. Mori further does not disclose such a serial to parallel conversion. Accordingly, claims 33-35 are believed allowable as patentable under 35 U.S.C. § 103(a) over Miller in view of Mori.

Conclusion

In light of the above amendments and remarks, claims 4, 6, 8-9 and 29-36 are now all believed to be in condition for allowance. Accordingly, reconsideration and allowance of these claims is respectfully requested.

Respectfully submitted,

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